NEWWOOD SOLUTIONS Ltd
Derby Office: 15 Kings Croft, Allestree, Derby, DE22 2FP.
Tel +44 (0)1332 721326

Reading Office: 13 Highfield Road, Tilehurst, Reading RG31 6YR.
Tel +44 (0) 118 9012298

Email: sales@newwoodsolutions.co.uk Web: www.newwoodsolutions.co.uk

CB-6335
PCIe TWO SITE INDUSTRY PACK CARRIER

USERS MANUAL

PCB Issue 3
FPGA Version 6335V4.0
8MHz or 32MHZ IP Clock

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Author: PJM/MRN

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/10/15	1.0	Use manual issue
09/10/14	2.0	Manual updated to show PCB at Issue 3 and latest FPGA version
12/11/19	2.1	Change from Hytec to Newwood Solutions for contact details

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1. INTRODUCTION

The 6335 is an Industry Pack Carrier card for the PCI Express bus. This card is used in a 'X1' PCI Express slot and can accommodate two single-width Industry Packs, which can be clocked at either 8MHz or 32MHz (individually selected). The PCI Express bus is converted to a 'local bus' by a bridge chip and then this local bus is interfaced to the Industry Pack (IP) Logic connectors by an FPGA. The IP interface supports Memory, I/O, ID and Interrupt access to the Industry Packs in the same way as is used in the 9010 IOC from Newwood Solutions. IP interrupts are mapped to the PCI Express bus. Driver support is available for both Windows and LINUX environments.

The PCIe interrupt can be enabled by writing to an on board register.

The interrupts INT0 and INT1 of both Industry Packs can be enabled on an individual basis.

PCB mounted LEDs flash to visually confirm completed IP access cycles to individual slots.

The card receives +12-volt and +3.3-volt power from the PCIe bus. From these, it produces +5 volts and -12 volts for the Industry Packs. Also, space is available for an optional DC-DC converter producing isolated +/- 12-volt supplies which can be used to power the 'front-end' of analogue Industry Packs such as the 8401 and 8402. These are selected by jumpers.

I/O connections are via a single 100-way right-angle connector with accepts a ribbon cable terminated in two 50-way SCSI-2 connectors. These I/O connections are compatible with Newwood Solutions range of DIN-rail mounted I/O termination and breakout assemblies. A cable adapter card 8924 can be used to allow connection to Hytec terminal blocks such as the 8901. This keeps the pinning the same on the terminal block.

A single-pole LEMO size 00250 socket is also fitted on the card bracket to allow an external TTL signal to be brought into the card. This can be used, via jumpers, to send a trigger or inhibit signal to each Industry Pack.

1.1 FPGA NOTES

This design uses the PEX 8311 Multi-purpose and Feature-Rich PCI Express Bridge
The design uses Local Bus Interface C Mode Signals (Non-Multiplexed) Mode pins MODE[1:0] (H20 & H19) are tied low on PCB.
The ROOT_COMPLEX# signal is pulled high (de-asserted) on the PCB. Thus the PEX 8311 acts as a PCI Express Endpoint device
The Carrier card Registers are accessed via the PCIe I/O area and are set out the same as the Hytec 9010 IOC.
The IP cards are accessed via the PCIe memory area which is remapped in the PLX IC at 0x01000000.
The only way of differentiating from I/O and memory space is via the address which is remapped to show I/O or memory.

2. INDUSTRY PACK MEMORY AREA

This area is 16 Mbytes wide, organised as 16-bit words. All accesses to Industry Pack resources are through this area, organised as follows:

Offset	Contents
0000000h-01FFFFEh	Memory area of Industry Pack A, 2Mbytes.
0200000h-03FFFFEh	Memory area of Industry Pack B, 2Mbytes.
0400000h-0BFFFFEh	Not used.
0C00000h-0DFFFFEh	Not used (spare).
0E00000h-0E00FFEh	Access to Industry Packs A-F I/O, ID and INT areas.

This last area is sub-divided as follows:

Offset	Contents
000h-07Eh	Industry Pack A I/O registers (64 bytes).
080h-0FEh	Industry Pack A ID registers (64 bytes).
100h-17Eh	Industry Pack B I/O registers (64 bytes).
180h-1FEh	Industry Pack B ID registers (64 bytes).
200h-5FEh	Not used
600h-7FEh	Not used
800h-8FEh	Industry Pack A INT registers (128 bytes, only 2 words used).
900h-9FEh	Industry Pack B INT registers (128 bytes, only 2 words used).
A00h- DFEh	Not used.
E00h-FFEh	Not used.

Note: for this last set of registers, an access at the base address requests the vector for IP Interrupt 0, and at base address plus two, the vector for Interrupt 1. All other addresses are not used.

3. Application Registers

The Carrier card Registers are accessed via the PCIe I/O area and are set out the same as the Hytec 9010 IOC.

Offset	Name	Description
0-6		Not used
8	INTS_LO	Read only access to the IP IRQ Status Register (4 bits)
A	INTS_HI	Read only access to the IP Error Status Register (3 bits)
C	MASK_LO	Read/write access to a mask register for IP IRQ sources
E	MASK_HI	Read/write access to a mask register for IP Error sources
10	IP_CLK	Read/write access the IP CLOCK SELECT register (2 bits)
12-1C		Not used.

3.1 INTERRUPTS LOW. (Offset 8h) [Read only]

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	X	X	X	X	INT REQ B1	INT REQ B0	INT REQ A1	INT REQ A0

Bits showing the states of two IP Interrupt output lines for all 2 industry packs.

3.2 INTERRUPTS HIGH. (Offset Ah) [Read only]

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	TIMO	X	X	X	X	X	X	ERR_B	ERR_A

Bits showing the state of IP Error outputs for all 2 industry packs plus one bit for the IP access timeout flag to allow an interrupt to be generated from it.

3.3 MASK LOW/HIGH (Offsets Ch, Eh)

Registers corresponding to Interrupt and Error flag bits in INTS LO & INTS HI above, to select which, if any, are permitted to produce a PC104+ processor interrupt. This interrupt is presented to the PC104+ card on PCI interrupt INTA#.

3.4 IP CLOCK SELECT. (Offset 10h)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	X	X	X	X	X	X	CKS_B	CKS_A

Bits to select the clock frequency for each Industry Pack. ‘1’ = 32MHz, ‘0’ = 8MHz.These bits all default to ‘0’ on power-up.

4. 6335 ID ROM

The ID configuration information held in the PROM is as detailed below.
The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Muef ID high byte	0080h	
Base+88	Murf ID low word	0300h	
Base+8A	Model number	6335h	
Base+8C	Revision	0301h	(This shows PCB Issue 3 and Xilinx at issue 1)
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	0000h	

Linux API
IOC9010 Blade/Hytec 5331/Hytec 6335/uTCA7002/7003 Linux API Functions including examples
Download
320KB
Linux Driver
IOC9010 Blade/Hytec 5331/Hytec 6335 Linux device drivers (both PCI and UART)

APPENDIX A

PCB JUMPERS

Jumper	Function/default setting
J1	Select Xilinx mode: must be IN.
J2	Connect LEMO input to STROBE on Industry Pack A.
J3	Connect LEMO input to STROBE on Industry Pack B.
J4-6	Not present.
J7	Connect isolated +12 volts to Industry Pack A IO signal paths.
J8	Connect isolated +12 volts to Industry Pack B IO signal paths.
J9	Connect isolated -12 volts to Industry Pack A IO signal paths.
J10	Connect isolated -12 volts to Industry Pack B IO signal paths.
J11	Connect isolated AGND to Industry Pack A IO signal paths.
J12	Connect isolated AGND to Industry Pack B IO signal paths.

APPENDIX B

CON 1 Connector – PL1 (100 way) on Issue 2 6335 Board

I/O Connector – 50 way on transition

Card 8304 Where this feeds ONE IP sites

Pin 8522	SCSI 50way		Pin 8522	SCSI 50way		Signal
1	1		*2*	26		IO1_P1
3	2		*4*	27		IO3_P2
5	3		*6*	28		IO5_P3
7	4		*8*	29		IO7_P4
9	5		*10*	30		IO9_P5
11	6		*12*	31		IO11_P6
13	7		*14*	32		IO13_P7
15	8		*16*	33		IO15_P8
17	9		*18*	34		IO17_P9
19	10		*20*	35		IO19_P10
21	11		*22*	36		IO21_P11
23	12		*24*	37		IO23_P12
25	13		*26*	38		IO25_P13
27	14		*28*	39		IO27_P14
29	15		*30*	40		IO29_P15
31	16		*32*	41		IO31_P16
33	17		*34*	42		Ext RST
35	18		*36*	43		TRIG/EBA OUT
37	19		*38*	44		Not Used
39	20		*40*	45		TRIG/EBA IN
41	21		*42*	46		GND
43	22		*44*	47		GND
45	23		*46*	48		GND
47	24		*48*	49		GND
49	25		50	*50*		GND

APPENDIX C

CON 1 Connector – PL1 (100 way) on Issue 3 6335 Board

I/O Connector – 50 way on transition

Card 8304 Where this feeds ONE IP sites

Pin Trans	Pin 8522	Signal	Pin Trans	Pin 8522	Signal
1	*2*	IO2_N1	26	*1*	IO1_P1
2	*4*	IO4_N2	27	*3*	IO3_P2
3	*6*	IO6_N3	28	*5*	IO5_P3
4	*8*	IO8_N4	29	*7*	IO7_P4
5	*10*	IO10_N5	30	*9*	IO9_P5
6	*12*	IO12_N6	31	*11*	IO11_P6
7	*14*	IO14_N7	32	*13*	IO13_P7
8	*16*	IO16_N8	33	*15*	IO15_P8
9	*18*	IO18_N9	34	*17*	IO17_P9
10	*20*	IO20_N10	35	*19*	IO19_P10
11	*22*	IO22_N11	36	*21*	IO21_P11
12	*24*	IO24_N12	37	*23*	IO23_P12
13	*26*	IO26_N13	38	*25*	IO25_P13
14	*28*	IO28_N14	39	*27*	IO27_P14
15	*30*	IO30_N15	40	*29*	IO29_P15
16	*32*	IO32_N16	41	*31*	IO31_P16
17	*34*	Not Used	42	*33*	Ext RST
18	*36*	Not Used	43	*35*	TRIG/EBA OUT
19	*38*	Not Used	44	*37*	Not Used
20	*40*	Not Used	45	*39*	TRIG/EBA IN
21	*42*	Not Used	46	*41*	GND
22	*44*	Not Used	47	*43*	GND
23	*46*	Not Used	48	*45*	GND
24	*48*	Not Used	49	*47*	GND
25	*50*	GND	50	*49*	GND

APPENDIX D

Cable Adapter Card 8924

A cable adapter card 8924 can be used to allow connection to Hytec terminal blocks such as the 8901. This keeps the pinning the same on the terminal block.