NEWWOOD SOLUTIONS Ltd
Derby Office: 15 Kings Croft, Allestree, Derby, DE22 2FP.
Tel +44 (0)1332 721326

Reading Office: 13 Highfield Road, Tilehurst, Reading RG31 6YR.
Tel +44 (0) 118 9012298

Email: sales@newwoodsolutions.co.uk Web: www.newwoodsolutions.co.uk

EC8513
Incremental Encoder Counter
INDUSTRY PACK

USERS MANUAL

PCB Issue 2
FPGA Version 8513V206

Document Nos.: EC8513/UTM/G/x/6.0
Date: 03/12/2019
Author: PM/MRN

Revision History

The following table shows the revision history for this document.

Date	Version	Change Notes
18/06/2002	1.0	Initial release.
03/09/2004	2.0	Chang to FPGA Version
06/12/2004	3.0	User manual does not mention that Interrupt Status register is used to clear interrupts.
02/02/2005	4.0	Change to FPGA. The index signal from the encoder may now clear the counter. Extra bits are declared in the Interrupt Mask Register to provide this functionality on a channel-by-channel basis.
03/07/2005	5.0	Change to FPGA. The index signal from the encoder now also clears the Mask register bit which had been set to allow this clear function to happen.
15/11/2018	6.0	Change from Hytec to Newwood Solutions for contact details

CRITICAL APPLICATIONS DISCLAIMER

THIS PRODUCT FROM NEWWOOD SOLUTIONS LTD USES COMPONENTS THAT ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, “CRITICAL APPLICATIONS”). FURTHERMORE, SOME COMPONENTS USED IN THIS NEWWOOD SOLUTIONS LTD PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR.

THE CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF NEWWOOD SOLUTIONS LTD PRODUCT IN CRITICAL APPLICATIONS.

CONTENTS

1. INTRODUCTION 4

2. PRODUCT SPECIFICATIONS 4

3. OPERATING MODE 4

4. APPLICATION REGISTERS 5

4.1 CONTROL & STATUS REGISTER (CSR) 5
4.2 ARM REGISTER (IP ADDRESS 1, OFFSET 02H) 5
4.3 IRQ STATUS REGISTER (IP ADDRESS 2, OFFSET 04H) 5
4.4 IRQ MASK REGISTER\INDEX CLEAR COUNTER MASK (IP ADDRESS 3, OFFSET 06H) 5

5. COUNTER REGISTERS 6

5.1 COUNTER REGISTERS 0 TO 3 6
5.2 (MEMORY ADDRESSES LSWORD 00-0CH, MSWORD 02-0EH) 6

COUNTER OPERATION 6

5.3 BASIC COUNTER OPERATION 6
5.3.1 Counter Inputs 6
5.3.2 Set up and enable interrupts. 6
5.3.3 ARM the counters 6
5.3.4 Reading counters on the fly 6
5.3.5 Interrupt handling 6

6. ID PROM 7

7. EPICS SOFTWARE DRIVER 7

APPENDIX A 8

APPENDIX B 9

APPENDIX C 10

1. INTRODUCTION

The Newwood Solutions IP-EC-8513 is a single-width Industry Pack that caters for four quadrature output incremental encoders. The signals Phase A, Phase B and Index from each of the four encoders are connected as TTL inputs at the I/O connector and operate on four 32 bit up/down counters which can be read or overwritten at any time. The maximum counting rate is 10MHz.
A companion unit, the 8906 DIN-rail mounted interface block can be used with this IP card (together with a suitable transition board) to provide RS-422 conversion for the encoder signals which then connect through individual D-type connectors to the plant.
An EPICs driver is available for this card.
The 8513 is a firmware variant of the IP-SC-8512 and has the following features :-

- 4 independent preset up/down counters
- Full 32 bits binary count capacity
- Each counter channel can count up/down from a pre loaded value
- Count rates from D.C. to 10MHz
- An ARM register allows individual channels to be enabled or inhibited
- Maskable interrupt generated by each channel on encoder index pulse
- Counter external inputs via transition board
- Counters can be read on the fly via a shadow register
- The ability to read the module identity, manufacturer, model, revisions and serial number from an onboard ID ROM.

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	4 encoders
Max. count:	32 bits.
Data format:	Binary
Max count rate:	10MHz
Input levels:	TTL compatible with jumper selectable 470Ω resistor pull-up or pull-down and positive edge clocking
Power:	+5V @ 180mA typical

3. Operating Mode

1. **Up/down Counter:** - the counter is reset to zero either using reset command (see CSR) or by writing 0 to the counter. Alternatively, a pre-set value can be loaded into the counter. The counter will count up or down according to Phase A/ Phase B input pulses when armed, and will wrap-round from ‘all-ones’ to ‘all-zeroes’ or vice-versa**. Note that due to the quadrature decoding method used, four counts are derived from each cycle of the encoder pulses, effectively quadrupling the resolution of the encoder. In other words, a 500 step-per-revolution encoder will result in 2000 counts per rotation.**

4. Application Registers

There are three application specific (I/O) registers; the CSR,

4.1 Control & Status Register (CSR)

Read/write register
Defines the interrupt vector V7-V0 and index status.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V7	V6	V5	V4	V3	V2	V1	V0	T				I4	I3	RS T/I2	I1

I1-4 Present State of Index bits 1-4
T Test. Writing a logic '1' increments/decrements all counters by one. Write only. [Depends on direction decode at the time].
RST Writing '1' to this bit clears all counters and registers in this channel.

4.2 Arm Register (IP address 1, offset 02h)

Read/write register.
Any bit that is set arms the relevant encoder counter.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												E3	E2	E1	E0

4.3 IRQ Status Register (IP address 2, offset 04h)

Read/write register.
Shows which channel index caused an interrupt.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
												Int3	Int2	Int1	Int0

4.4 IRQ Mask Register\Index Clear Counter Mask (IP address 3, offset 06h)

Read/write register.
Any bit that is set in the range 0-3 allows an index signal on the respective channel to generate IRQ.
In version 8513v205 and up of the firmware any bit that is set in the range 4-7 allows an index signal on the respective channel to clear the corresponding 32-bit counter.
In version 8513v206 of the firmware the index signal also clears the Index Clear Counter Mask bit

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								ICM3	ICM2	ICM1	ICM0	M3	M2	M1	M0

5. Counter Registers

5.1 Counter Registers 0 to 3

5.2 (Memory addresses LSWord 00-0Ch, MSWord 02-0Eh)

The counter registers may be read at memory addresses 00-0Ch for the least significant words

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

and 02-0E for the most significant words.

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

Writing to the appropriate addresses, having first disabled counting by disarming the counter can set the counter value.

Counter OPERATION

5.3 Basic Counter Operation

5.3.1 Counter Inputs

The counters can be clocked either internally using the Test clock or externally via the transition board see appendix B for connections. Note that the Test Clock will increment or decrement the corresponding counter by one depending on the current state of the quadrature decoding logic and is therefore indeterminate.

5.3.2 Set up and enable interrupts.

If interrupts are to be used then the interrupt vector must be loaded in to the top byte of the CSR register. Enable the interrupt for the index signal of the relevant counter by writing 1 to the respective bit in the IRQ Mask register.

5.3.3 ARM the counters

To arm the counters, write a one in to the relevant bit of the ARM register. Note that the hardware ARM IN/ ARM OUT system used on the 8512 is not implemented in this card.

5.3.4 Reading counters on the fly

All counters have their current count stored in a shadow register. This allows readouts to be taken in parallel to the acquisition of new data.

5.3.5 Interrupt handling

The interrupt handling routine should clear the interrupt by clearing the relevant bit in the IRQ Status register as soon as possible; this is achieved by reading the IRQ Status register to see which counter channel/s have caused the interrupt and then zero the corresponding bit(s) in the IRQ Status register.

6. ID PROM

The 8513 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

The byte addresses of the ID PROM are as below: -

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Murf ID high byte	0080h	
Base+88	Murf ID low word	0300h	
Base+8A	Model number	8513h	
Base+8C	Revision	2206	This shows PCB Issue 2 and Xilinx V206means Xilinx at issue 6 for PCB issue 2.
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	0000h	
Base+9A	Serial Number	xxxxdec	

7. EPICS Software Driver

EPICS software driver written for the 8513 Quadrature Incremental Encoder Counter Industry Pack on 8002/8802 Carrier Board with 8304 Transition Board.

For down loads go to:
http://www.newwoodsolutions.co.uk/Default.aspx

APPENDIX A

PCB JUMPER (settings for PCB Issues 1 and 2)

J1 Factory set

J2 Terminate external counter clocks to GND or 3Volts.
Terminate to GND = pins 1 & 2 Terminate to 3Volts = pins2 & 3.

J3 Terminate external control lines ARM IN and ARM OUT to GND or 3Volts (NOT USED)
Terminate to GND = pins 1 & 2 Terminate to 3Volts = pins2 & 3.

J4 to J10 not used

APPENDIX B

I/O Connector – 50 way on 8513 Counter Board

Pin	Signal	Pin	Signal
1	Ch 1 Phase A	26	GND
2	GND	27	Ch 4 Phase B
3	Ch 1 Phase B	28	GND
4	GND	29	Ch 4 Index
5	CH 1 Index	30	GND
6	GND	31	Reserved I/P16
7	Reserved I/P4	32	GND
8	GND	33	Spare 1
9	Ch 2 Phase A	34	GND
10	GND	35	N.C.
11	Ch 2 Phase B	36	GND
12	GND	37	Spare 2
13	Ch 2 Index	38	GND
14	GND	39	N.C.
15	Reserved I/P8	40	GND
16	GND	41	N.C.
17	Ch 3 Phase A	42	GND
18	GND	43	N.C.
19	Ch 3 Phase B	44	GND
20	GND	45	N.C.
21	Ch 3 Index	46	GND
22	GND	47	N.C.
23	Reserved I/P12	48	GND
24	GND	49	N.C.
25	Ch 4 Phase A	50	GND

APPENDIX C
HYTEC TRANSITION CARD CONNECTIONS

I/O Connector – 50 way on transition

Card 8202 where this feeds ONE IP sites

Pin	Signal	Pin	Signal
1	GND	26	Ch 1 Phase A
2	GND	27	Ch 1 Phase B
3	GND	28	Ch 1 Index
4	GND	29	Reserved IP4
5	GND	30	Ch 2 Phase A
6	GND	31	Ch 2 Phase B
7	GND	32	Ch 2 Index
8	GND	33	Reserved IP8
9	GND	34	Ch 3 Phase A
10	GND	35	Ch 3 Phase B
11	GND	36	Ch 3 Index
12	GND	37	Reserved IP12
13	GND	38	Ch 4 Phase A
14	GND	39	Ch 4 Phase B
15	GND	40	Ch 4 Index
16	GND	41	Reserved IP16
17	N.C.	42	N.C.
18	GND	43	N.C.
19	N.C.	44	N.C.
20	GND	45	N.C.
21	N.C.	46	N.C.
22	N.C.	47	N.C.
23	N.C.	48	N.C.
24	N.C.	49	N.C.
25	N.C.	50	N.C.