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SI-8515
Octal RS-232
INDUSTRY PACK

USERS MANUAL

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Revision History

The following table shows the revision history for this document.

Date	Version	Change Notes
04/08/2002	1.0	Initial release.
22/09/2006	1.1	ENI Enable Infra-red mode. Read/write removed from control register
15/11/2018	1.2	Change from Hytec to Newwood Solutions for contact details

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1. Product Description

The Newwood Solutions IP-SI-8515 is a single-width Industry Pack that provides 8 serial interface lines with the following characteristics:-

- 8 independent RS-232 UART channels
- 64 byte Transmit and Receive FIFOs
- Transmit and Receive FIFO level counters
- Programmable Tx and Rx FIFO Trigger Levels
- Automatic RTS/CTS Flow Control
- Automatic Xon/Xoff Software Flow Control with Status Indication
- Programmable Data Rate with Prescaler
- Up to 6.25 Mbps Serial Data Rate
- Single Interrupt Output for all 8 UARTs
- Global Interrupt Source for all 8 UARTs
- Simultaneous UART channel initialisation

2. Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	8
Max. baud rate:	921.6kbps with internal clock.
Data format:	Binary/ASCII
Input/Output levels:	RS-232
Internal clock:	14.7456MHz oscillator
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 400mA typical
Fuses:	F1 1A – connects +12V to I/O connector
	F2 1A – connects –12V (not used)
Jumpers:	J1 Boot jumper allows FPGA to load.
	J2, J3 not used.

3. Application Registers

There are a number of application specific (I/O) registers. All are word addressed.

Interrupt Register (IP address 0)

Read/write register defines the vector V7-V0, Read only interrupt source U7-U0

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V7	V6	V5	V4	V3	V2	V1	V0	U7	U6	U5	U4	U3	U2	U1	U0

V0-7 Interrupt vector to be used during IACK
U0-7 Any bit which is set indicates the interrupting UART

Interrupt Source Registers 1 (IP address 1)

Read only register
Indicate the source of each interrupt from UART0 to 7 . Bits 8-15 are 0..

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								U21	U20	U12	U11	U10	U02	U01	U00

Interrupt Source Registers 2 (IP address 2)

Read only register
Indicate the source of each interrupt from UART0 to 7 . Bits 8-15 are 0..

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								U50	U42	U41	U40	U32	U31	U30	U22

Interrupt Source Registers 3 (IP address 3)

Read only register
Indicate the source of each interrupt from UART0 to 7 . Bits 8-15 are 0..

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								U72	U71	U70	U62	U61	U60	U52	U51

Timer Control Register (IP address 4)

Read/write register.
CS-Clock Select S/R-Single/Retrigger SS-Start/Stop IE-Timer Interrupt Enable

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								0	0	0	0	CS	S/R	SS	IE

Timer Control Register (IP address 5)

Read/write register.
CS-Clock Select S/R-Single/Retrigger SS-Start/Stop IE-Timer Interrupt Enable

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								0	0	0	0	0	0	0	0

Timer Counter Register LS (IP address 6)

Read/write register.
Timer counter data register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								D7	D6	D5	D4	D3	D2	D1	D0

Timer Counter Register MS (IP address 7)

Read/write register.
Timer counter data register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								D7	D6	D5	D4	D3	D2	D1	D0

8x Mode Register (IP address 8)

Read/write register.
Logic 0 sets 16x sampling. Logic 1 sets 8x sampling

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	U7	U6	U5	U4	U3	U2	U1	U0

Reserved Register (IP address 9)

Read only register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reset Register (IP address A)

Resets are write only
R0-7 reset UART0-7

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Sleep Register (IP address B)

S0-7 set UART0-7 into sleep mode Read/write register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	S7	S6	S5	S4	S3	S2	S1	S0

Device Revision Register (IP address C)

(UART device revision – read only)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Device ID Registers (IP address D)

(UART device ID – read only)

D07	D06	D05	D04	D03	D02	D01	D00	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	I7	I6	I5	I4	I3	I2	I1	I0

Control Register (IP address E).

(Read/write)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
IRQ	IEN	0	0	0	0	0	RST	0	0	0	0	0	0	0	WA

IRQ Any IRQ which is set and masked on sets this status bit. Read only
IEN Interrupt Enable. Masks on IRQ when set to a 1. Read/write
RST Writing a 1 generates a reset to the UART device. Write only.
WA Setting this to a 1 enables writing to all UARTs in parallel. Read/write

4. UART Channel Configuration Registers

(Memory word addresses 00-7F)

Each UART has a set of 16 configuration registers at addresses 0x,1x,2x….7x as follows:

Address	Reg	R/W	D07	D06	D05	D04	D03	D02	D01	D00
0 (LCR7=0)	RHR	R	R7	R6	R5	R4	R3	R2	R1	R0
0 (LCR7=0)	THR	W	T7	T6	T5	T4	T3	T2	T1	T0
0 (LCR7=1)	DLL	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1 (LCR7=1)	DLH	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	IER	R/W	CTS	RTS	Xon	0	MSIE	RSIE	TEIE	RDIE
2	ISR	R	FE	FE	FC	Xoff	IS3	IS2	IS1	IS0
2	FCR	W	RFT	RFT	TFT	TFT	DMA	TFR	RFR	FE
3	LCR	R/W	DE	STB	SP	EP	PE	SB	WL1	WL0
4	MCR	R/W	BP	IRE	XA	ILE	OP22	OP12	RTS	DTR
5	LSR	R/W	RFE	TSRE	THE	RxB	RxFE	RxPE	RxO	RDR
6	MSR	R	CD	RI	DSR	CTS	DCD	DRI	DDS	DCT
6	MSR	W	DL3	DL2	DL1	DL0				
7	SPR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8	FCTR	R/W	TR1	TR0	AE	IIR	H3	H2	H1	H0
9	EFR	R/W	ACE	ARE	SCS	EN	SF3	SF2	SF1	SF0
A	TFCNT	R	D7	D6	D5	D4	D3	D2	D1	D0
A	TFTRG	W	D7	D6	D5	D4	D3	D2	D1	D0
B	RFCNT	R	D7	D6	D5	D4	D3	D2	D1	D0
B	RFTRG	W	D7	D6	D5	D4	D3	D2	D1	D0
C	XCHAR	R							XOnI	XOfI
C	XOFF1	W	D7	D6	D5	D4	D3	D2	D1	D0
D	XOFF2	W	D7	D6	D5	D4	D3	D2	D1	D0
E	XON1	W	D7	D6	D5	D4	D3	D2	D1	D0
F	XON2	W	D7	D6	D5	D4	D3	D2	D1	D0

RHR – Receive Holding Register THR – Transmit Holding Register
DLL – Div Latch Low DLH – Div Latch High
IER - Interrupt Enable Register ISR - Interrupt Status Register FCR – FIFO Control Register
LCR – Line Control Register MCR – Modem Control Register LSR – Line Status Register
MSR – Modem Status Register SPR - Scratch Pad Register
FCTR EFR - Enhanced Function Register
TFCNT- Transmit FIFO Counter TFTRG – Transmit FIFO Trigger Level
RFCNT – Receive FIFO Counter RFTRG – Receive FIFO Trigger Level
XOFF1 – Xoff Character 1 XOFF2 – Xoff Character 2
XON1 – Xon Character 1 XON2 – Xon Character 2

5. ID PROM

The ID data byte addresses are as below:-

00	ASCII 'VI'	02	ASCII 'TA'
04	ASCII '4 '	06	Mrf ID high byte
08	Mrf ID low word	0a	Model number
0c	Revision	0e	UART
10	Driver ID	12	Driver ID
14	Flags (8MHz)	16	No of bytes used
18	Not used	20	Not used
22	Serial no. high word	24	Serial no. low word

6. IP-SI 8515 I/O Connector

Connector: 50 way

Pin	Signal	Pin	Signal
1	GND	26	GND
2	Tx0	27	Tx5
3	Rx0	28	Rx5
4	/RTS0	29	/RTS5
5	/CTS0	30	/CTS5
6	GND	31	GND
7	Tx1	32	Tx6
8	Rx1	33	Rx6
9	/RTS1	34	/RTS6
10	/CTS1	35	/CTS6
11	GND	36	GND
12	Tx2	37	Tx7
13	Rx2	38	Rx7
14	/RTS2	39	/RTS7
15	/CTS2	40	/CTS7
16	GND	41	GND
17	Tx3	42	+12V Fused
18	Rx3	43	CD0 (TTL input)
19	/RTS3	44	CD1 (TTL input)
20	/CTS3	45	CD2 (TTL input)
21	GND	46	CD3 (TTL input)
22	Tx4	47	CD4 (TTL input)
23	Rx4	48	CD5 (TTL input)
24	/RTS4	49	CD6 (TTL input)
25	/CTS4	50	CD7 (TTL input)

7. Connections to IP-SI-8515 using the TB8304 Straight-through Transition Board

SCSI Pin	RS-232	SCSI Pin	RS-232
1	/TX0	26	GND
2	RTS0	27	/RX0
3	GND	28	CTS0
4	/RX1	29	/TX1
5	CTS1	30	RTS1
6	/TX2	31	GND
7	RTS2	32	/RX2
8	GND	33	CTS2
9	/RX3	34	/TX3
10	CTS3	35	RTS3
11	/TX4	36	GND
12	RTS4	37	/RX4
13	GND	38	CTS4
14	/RX5	39	/TX5
15	CTS5	40	RTS5
16	/TX6	41	GND
17	RTS6	42	/RX6
18	GND	43	CTS6
19	/RX7	44	/TX7
20	CTS7	45	RTS7
21	+12V	46	GND
22	/CD1 (TTL)	47	/CD0 (TTL)
23	/CD3 (TTL)	48	/CD2 (TTL)
24	/CD5 (TTL)	49	/CD4 (TTL)
25	/CD7 (TTL)	50	/CD6 (TTL)

NOTES

1. /CD0-7 ARE TTL CARRIER DETECT OR GENERAL PURPOSE INPUTS
2. WHEN USING RS-485 HALF-DUPLEX CONNECT ONLY TX+ AND TX-