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IP-WD-8530/8630
IP-WATCHDOG
INDUSTRY PACK

USERS MANUAL

PCB Issue 1.0
Firmware Version WD8530V103

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/11/12	1.0	Initial release
24/09/13	1.1	Content of ID Rom has change at Customer request (see CH333)
18/05/16	1.2	The manual states to read the input register first a logic input "1" must be written to the output register. It has been discovered that if a logic input "1" or a logic input "0" is written, that the same result is seen when reading the input register contents. Important Note 2 has been added to manual to highlight this.
04/08/17	1.3	L is Write only. Writing a logic 0 to the Load bit has no effect.
15/10/17	1.4	Change company info to show Newwood Solutions Ltd Clear Timer counter load register when in reset mode and SYSRESET is set. Clear SYSRESET when zero written to SYSRESET bit in Timer Cntl reg.
27/11/17	1.5	Put in description for pins in I/O pin wiring table
02/08/18	1.6	Put in power consumption figures
10/11/19	1.7	The 8630 has added functionality over the 8530 by adding the system reset functionality of the Hytec VDS2801-R VME module.
26/02/20	1.8	Incorrect part number used should be VDS2081-R

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CONTENTS

1. INTRODUCTION

The Newwood Solutions IP-WD-8530/8630 is a single-width Industry Pack that provides a watchdog timer, power supply monitoring, temperature monitoring and general purpose TTL I/O with the following characteristics:

- Programmable Periodic or Watchdog Timer with interrupt and TTL outputs.
- Timer programmable from 1 millisecond to 65.536 seconds.
- Three external timer outputs:
  VMEbus SYSRESET*
  Timer = zero
  Toggle on zero
- Four range; +24V -24V, +48V or -48V auxiliary voltage monitor
- Three power supply monitors; +5V, +12V and -12V for internal or external supplies.
- Programmable Temperature Monitor/Thermostat.
- Open collector TTL outputs from Timer and Monitors with programmable polarity.
- Eight TTL compatible digital I/O lines
- Interrupts available from all I/O, Timer and Monitor Functions

1.1 WP-IP-8630 Added Functionality

The 8630 includes the power up system reset functionality of the Hytec VDS2081-R VME module.
This function ensures that a crate reset is generated for a fixed duration (160ms +/- 20%) whenever the crate is powered up. The unit archives this by generating a reset on the SYSRESET* line of the P1 connector when the power is asserted.
The circuitry also ensures that intermittent power-down and power-up will generate reset for at least 80ms.

2. Product Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Digital I/O:	8 lines individually programmable as input or output. Outputs are open collector with I0k pull-up resisters, 48 mA sink capability. Input line interrupt polarities individually programmable.
Timer:	16-bit programmable timer. 1kHz input from IP Clock. Down counter, interrupt and TTL output when zero. On the fly counter re-load for extending time-out period. Watchdog and Periodic modes.
Watchdog Mode:	Time-out halts operation. VMEbus SYSRESET* on time-out. 1 millisecond to 65.536 seconds range.
Periodic mode:	Interrupts and TTL outputs at regular intervals. Toggle output for 50% duty cycle signals. Toggle output range 2 millisecond to 131.072 second cycles.
SYSRESET*:	VMEbus compliant SYSRESET* output. 48 mA sink, open collector driver, 256 millisecond duration. IP retains time-out indicator during SYSRESET* cycle.
Power ON SYSRESET* (8630 only) :	At crate power up the SYSRESET* is generated for 160ms +/-20% Intermittent power-down and power-up will generate reset for at least 80ms.
Monitors:	Three internal or external power supply voltage monitors. One external auxiliary monitor with four different taps. Temperature Monitor, -55 to +125 Celsius range. 0.5 deg C accuracy. All monitors generate interrupts and TTL outputs. 100 Hz low pass filter on Voltage Monitors.
Tolerance:	+5V, +12V and -12V volt monitors ANSI/IEEE STD 1014 1987 Rule 6.2.1 +48V, +24V -24V and -48V volt monitors: 10%.
Interrupts:	Single programmable interrupt vector. 8 digital I/O interrupt sources. One timer interrupt source. One temperature interrupt source. Four voltage monitor sources.
Operating temp:	0 to 45 deg C ambient
Current draw:	+5V highest current draw measured during test is 120mA. +5V average current draw is approx. 105mA +12V highest current draw measured during test is 15mA. -12V highest current draw measured during test is 5mA.

3. Application Registers For IP Watchdog

The WD8530 has sixteen I/O registers. These can be classified into five groups:
1) General Purpose I/O.
2) Watchdog Timer.
3) Power Monitors.
4) Temperature Group.
5) Interrupts.
6) FPGA Version
The following section describes these registers in detail.

Application Register Table

Byte Addressing		**Word Addressing**		**16 Bit Application Registers**
Hex	***Dec***	***Hex***	***Dec***	
0	0	0	0	Output (8bits r/w)
2	2	1	1	Input (8 bit Read-back read only)
4	4	2	2	Monitor output Polarity (6 bit r/w)
6	6	3	3	Monitor Over voltage (6 bit read only)
8	8	4	4	Timer Load (16 bit r/w)
A	10	5	5	Timer Value (16 bit read only)
C	12	6	6	Timer Control (5 bits r/w)
E	14	7	7	Thermometer Data (1 bit r/w)
10	16	8	8	Thermometer Control RST/ (1 bit r/w)
12	18	9	9	Interrupt Sources (16 bits read only)
14	20	A	10	Interrupt polarity (16 bits some r some r/w)
16	22	B	11	Interrupt Enable (16 bits r/w)
18	24	C	12	Interrupt Clear (16bits read only)
1A	26	D	13	Interrupt Pending (16 bits read only)
1C	28	E	14	Interrupt Vector (8 bits r/w)
1E	30	F	15	NOT USED
20	32	10	16	FPGA Version Number (16 bits read only)

3.1 General Purpose O/I

3.1.1 General Purpose Output Register (I/O Address 0)

Read/write register 8 bits

The Output register is a latching register that is used to drive the I/O lines. Writing a '1' to this register will set the corresponding I/O line to a TTL high (+5 volts). Writing a zero will produce a TTL low (0 volts). This register is both read and write. Data read from this register is from the output latch, NOT the I/O line. This is useful for verification of previously written data and direction configuration. The power up default value of the output register bits is '1' (+5 volts). There are eight bits in the Output Register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	IO8	O7	IO6	IO5	IO4	IO3	IO2	IO1

3.1.2 General Purpose Input Register (I/O Address 2)

Read register 8 bits

The Input register reads the state of the eight I/O line regardless of data direction.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1

The I\O lines are direction configurable on a bit by bit basis. Writing a '1' to the corresponding bit in the Output Register turns off the TTL open collector buffer/driver. Incoming signals will overpower the l0k pull-up resistor and force the I/O line's state. The incoming data is then read from the Input Register at the same bit location.

Important Note 1
To receive Input data a loigc '1' must be written to the Output Register bit corresponding to each I/O line used for input.

Important Note 2
The Inputs may still see changes if a logic '0' is written to the output register. This will occur when the input signal is sufficient to cause the output protection of the output buffer to shut down its open collector output.

3.2 The Power Monitor Group

The WD8530 is equipped with four power monitors. Three of the monitors can monitor onboard or external (via a fuse) +5, +12 and -12 volt power sources. The fourth auxiliary monitor is external only and provides taps for monitoring one of four common voltages +48, +24, -24 or -48 volts. The power monitor group consists of two registers the Monitor Output Polarity Register and the Over-voltage Register. The bits in these registers are arranged in an overlapping order consistent with the interrupt scheme.

Links determine whether the onboard or the fused external power supply is to be monitored as shown by the table below.

Onboard Volts	Link Setting IN
+5	E1-2
+12	E3-4
-12	E5-6

Important Note
The External voltages should not be applied when the links are in.

Links determine the polarity of the auxiliary polarity monitors as shown in table below. Only two shunts are used at a time in these four locations.

Auxiliary Volts	Link Setting	
	Upper	Lower
+24 or +48	E9-10	E11-12
-24 or -48	E13-14	E15-16

Important Note
Only one auxiliary tap can be connected at a time see table above i.e. either to monitor a negative or positive voltage.

3.2.1 Power Monitor Voltage Limits

The WD8530 Voltage Monitors assert alerts if a voltage drifts outside the acceptable range. To prevent false alarms the WD8530 is guaranteed NOT trip when a supply is within tolerance, The +5, +12 and -12 volt supply tolerances are defined by the VMEbus voltage specifications. (ANSI/IEEE STD l0l4 1987 Rule 6.2.1). The 24 and 48 volt ranges are set at +/-10%. A complete table of voltage monitor limits is shown below.

Range (V)	Alert (V)	Monitored Voltage Tolerance	Alert (V)	Range (V)
4.825	4.590	+5V VME Spec	5.300	5.572
11.59	11.20	+12V VME Spec	12.65	13.30
-12.65	-13.30	-12V VME Spec	-11.59	-11.02
21.60	20.55	+24V +/-10%	26.40	27.75
-26.40	-27.75	-24V +/-10%	-21.60	-20.55
43.20	41.09	+48V +/-10%	52.80	55.51
-52.80	-55.51	-48V +/-10%	-43.20	-41.09

3.2.2 Monitor Output Polarity Register (I/O Address 4)

Read/write register 6 bits

The Monitor Output Polarity register selects the driver polarity for TTL *status* output signals. A logic '0' selects an active low output (Asserted = 0 volts), and a logic '1' selects an active high output (Asserted = 5 volts). Each status output is configurable on a bit by bit basis. There are six functional bits in the Monitor Output Polarity register. Each of the four power monitors has a TTL status output, additionally the watchdog timer, and the thermostat monitor both have TTL status outputs.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	PTH	PAX	PTI	PM12	PP12	PP05

PP05 +5V monitor '1'=active high '0'=active low.
PP12 +12V monitor '1'=active high '0'=active low.
PM12 -12V monitor '1'=active high '0'=active low.
PTI Timer=zero '1'=active high '0'=active low..
PAX Auxiliary voltage monitor '1'=active high '0'=active low.
PTH Thermostat monitor '1'=active high '0'=active low.

3.2.3 Over Voltage Register (I/O Address 6)

Read register 6 bits

The Over Voltage register indicates if power monitors have exceeded their nominal range. Each power monitor has an Over Voltage bit.
Similarly the Temperature/Thermostat monitor uses a bit in the Over Voltage register to indicate temperatures above the user defined limits.
A logic '1' indicates the voltage magnitude (or temperature) exceeds the nominal range.
Power monitor conditions can be directly read from the INTD register. See the interrupt section for complete details. In the INTD register a logic '1' indicates a fault. The INTD information used in conjunction with the Over Voltage information can determine if the input voltage is high, low or in bounds.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	TH	AX	-	M12	P12	P05

P05 +5V monitor '1'=voltage high '0'=OK or low.
P12 +12V monitor '1'=voltage high '0'=OK or low..
M12 -12V monitor '1'=voltage high '0'=OK or low.
AX Auxiliary voltage monitor '1'=voltage high '0'=OK or low.
TH Thermostat monitor '1'=temp high '0'=OK or low.

3.3 The Timer Group

The Watchdog timer is a 16 bit binary down counter that decrements once every millisecond. The time period can be set from 1 millisecond to 6536 Seconds. The WD8530 has two timer modes Watchdog and Periodic. In Watchdog mode the counting stops when the timer value reaches zero. In Periodic mode the counter is automatically re-loaded and re-started when the timer value reaches zero. In Watchdog mode the WD8530 can assert system interrupts, drive TTL outputs or VMEbus SYSRESET*. In Periodic mode the WD8530 can produce periodic system interrupts, TTL output signals and a toggling TTL output for use as a clock.

The Timer Group consists of three registers: The Timer Load register, the Timer Count register and the timer Control register. For timer I/O three TTL level open collector outputs are provided:
Timer = zero Status Output (TIZSO),
Timer Periodic Status Output (TIPSO),
VMEbus compliant System Reset (SYSRESET*).

3.3.1 Timer Load Register (I/O Address 8)

Read/write register 16 bits

The Timer Load Register is a 16 bit double buffer latch. Data in this register is loaded (or re-loaded) into the timer by strobing the L bit in the Timer Control Register. The Timer Load Register is both read and write accessible. The power on reset value, and post SYSRESET* value is 0x0000.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LT15	LT14	LT13	LT12	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0

3.3.2 Timer Value Register (I/O Address A)

Read register 16 bits

The Timer Value Register contains the current timer value. The counter is "broadside loaded" from the Timer Load Register by setting the L bit in the Timer Control Register.
The reading of the Timer Value Register is via a shadow register which allows the timer value to be continuously read.
The power on reset value, and post SYSRESET* value, is 0x0000.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

3.3.3 Timer Control Register (I/O Address C)

Read/write register 5 bits

The Timer Control Register has five bits that control timer operation. They are referred to by the acronyms L, RS, PM, RE, & RF.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	RF	RE	PM	RS	L

L: The Load bit transfers data from the Timer Load register to the timer down counter. This bit can be used to initialize or reload the counter on the fly. Writing a logic '1' to the L bit loads the counter. L is Write only. Writing a logic 0 to the Load bit has no effect.

RS: The Run/Stop bit starts and stops the counter. Writing a logic '1' to the Run/Stop bit starts the counter. Writing a logic '0' to the Run/Stop bit halts the timer.

PM: The PM bit switches the counter into periodic mode. In Periodic mode the timer is automatically reloaded and restarted every time it reaches zero. This can be used to produce TTL pulses and interrupts at regular intervals from 1 millisecond up to 65 seconds. Also there is a toggling TTL output that can produce, 50% duty factor clock signals with periods form 1 milliseconds to 65 seconds. The opposite, or complement, of Periodic mode is Watchdog mode. In Watchdog mode counting halts when the timer value reaches zero, the timer does not reload or restart. Enabling SYSRESET* forces the WD8530 into Watchdog mode. Writing a logic '1' to the PM bit selects Periodic Mode. Writing a logic '0' to the PM bit selects Watchdog mode. This bit is read write. The power on default value is logic '0' (i.e. Watchdog mode).

RE: The Reset Enable bit enables the VMEbus SYSRESET* output. Additionally it configures the timer, after zero is reached, to sustain the SYSRESET* signal for its specified 256 millisecond duration. This bit should be approached with caution. For safety the SYSRESET* output must be externally hardwired, via the I/O connector, to the VME backplane. The IP cannot drive SYSRESET* back through the carrier. Setting this bit also inhibits the PM function, forcing the IP into Watchdog mode. The RE bit is read write. Writing a logic '1' to this bit enables SYSRESET* output. Writing a logic '0' to the RE bit disables the SYSRESET* output. The power on default value for RE bit is logic '0' (i.e. SYSRESET* disabled). After a SYSRESET* cycle this bit is automatically cleared.
During the SYSRESET* blackout, the FPGA will remain active. The I/O and monitor systems will remain active. TTL output signals from the I/O lines and monitors can still be used during SYSRESET* blackout.

RF: The Reset Flag. This bit indicates that the SYSRESET* output has been asserted in the past. When the SYSRESET* feature is utilized, this bit is set to logic '1' when the SYSRESET* signal is asserted. The RF flag will stay set through the reset cycle and should be polled in the boot routine to determine if the WD8530 caused a reset. When set the RF flag disables both IRQ signals. This prevents Interrupts from being asserted until RF is cleared during re-boot. RF does not change the state of any of the Interrupt Registers. Any pending interrupts will be asserted as soon as RF is cleared.

Important Note

To use the SYSRESET* function the link E7-8 must be removed to disconnect the IP from the RESET* signal on the IP logic interface.

3.4 The Temperature Monitor Group

The WD8530 is equipped with a Maxim DS1620 Digital Thermometer/Thermostat IC. The DS1620 provides on-demand temperature data and thermostat monitors. Temperature is measured at the IC package itself, no external sensor is used. The IC is mounted near the centre of the IP card away from high profile components for good air flow and integration of board level temperature. Thermostat trip levels are user programmable. Serial access to the DS1620 is provided via two registers the Thermo Data Register and the Thermo Control Register. These are both *single* bit registers that connect to the DS1620's DQ and RST pins respectively. The DS1620 is serially accessed by reading and writing to these registers. Low level timing assistance and handshaking is automatically provided by the IP card. The DS1620 and its protocols are described in the Maxim DS1620 data sheet.

The serial data bit DQ is read write and bi-directional. The DS1620 serial interface is bi-directional. Direction is under software control. Caution must exercised to prevent data collision on this line. The RST* bit is write only. The T_{high} and T_{low} pins of the DS1620 are monitored by the WD8530 for out of bound conditions. Fault conditions trigger TTL level outputs and can assert system interrupts.

3.4.1 Thermometer Data Register (I/O Address E)

Read/write register 1 bits

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DQ

3.4.2 Thermometer Control Register (I/O Address 10)

Read/write register 1 bits

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RST/

3.5 The Interrupt Group

The WD8530 can generate system interrupts for any of its function groups. For highest priority, the power supply monitors, timer, and thermostat generate interrupts on IP IRQ level 1. The General purpose I/0 lines generate interrupts on IP IRQ level 0. The structure consists of five overlaying registers that monitor and qualify interrupt sources. The sixth register is the user programmable interrupt vector.
The WD8530's interrupt circuitry is based setting and clearing interrupt latches. When an interrupt condition is detected the interrupt latch is set.
The interrupt source state can be read from the INTD Register. Next the polarity circuit qualifies the signal for rising or falling edge. Polarity if applicable can be selected with the INTP Register. The signals are then passed through an edge detector which sets the interrupt latch. The latch contents can be read from the INTPEN Register. The interrupt latch will remain set until cleared with the INTCLR Register, regardless of changes in the interrupt source state. To pass the interrupt on the host the INTEN bit must be set. When the latch is set and INTEN is set an interrupt request will be asserted. The INTEN bit is guaranteed to be reset on power up (i.e. interrupts disabled). However the interrupt latches should be cleared during initialization because transient conditions during power up may be detected and latched.

3.5.1 INTD: The Interrupt Data Register (I/O Address 12)

Read register 16 bits

There are fourteen functional interrupt sources on JP-Watchdog: the eight I/O lines the timer, the four power monitors, and the thermostat. This register provides direct access to interrupt sources. The INTD inputs are transitory. This allows the sources to be polled and ISRs to verify that corrective action has been effective before re-enabling interrupts. Faults on the power monitors, timer = zero, and temperature out of bounds are indicated by logic ‘1’. Acceptable conditions on the power monitors, timer = zero and temperature monitor are indicated by logic ‘0’. The power on default value for the Timer is 0x0000, therefore the TI bit in the INTD register will default to Logic ‘1’. The I/O lines indicate the state of the I/O lines when polled.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I8	I7	I6	I5	I4	I3	I2	I1	-	-	TH THSO	AX AUXSO	TI TIZSO	M12 M12SO	P12 P12SO	P05 P05SO

3.5.2 INTP: The Interrupt Polarity Register (I/O Address 14)

Read\write register 16 bits

All of the WD8530 general purpose I/O lines can be used as interrupt sources. The Interrupt Polarity Register configures interrupts for rising or falling edges. Each I/O line's polarity is configurable on a bit by bit basis. Writing a logic ‘0’ causes the interrupt to be triggered a falling edge. Writing a logical ‘1’ causes the interrupt to be triggered rising. The power on default for Interrupt Polarity bits is ‘0’, or falling edge.
Polarity bits for the voltage monitor, timer and thermostat functions are not user selectable.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I8	I7	I6	I5	I4	I3	I2	I1	-	-	TH	AX	TI	M12	P12	P05

3.5.3 INTEN: The Interrupt Enable Register (I/O Address 16)

Read\write register 16 bits

The Interrupt Enable register masks all the interrupt sources. Writing a logic ‘1’ to the register enables system interrupt. Writing a logical ‘0’ disables the interrupt. The INTEN bit is guaranteed to be reset on power up (i.e. interrupts disabled). However, the interrupt latches should be cleared during initiation because transient conditions during power up may be detected and latched. All interrupt sources can be enabled on a bit by bit basis.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I8	I7	I6	I5	I4	I3	I2	I1	-	-	TH	AX	TI	M12	P12	P05

3.5.4 INTCLR: The Interrupt Clear Register (I/O Address 18)

Write register 16 bits

This register clears the interrupt latch. Each bit is connected to the reset of the corresponding interrupt latch. Writing a ‘1’ to a bit clears the latch. Writing a ‘0’ to a bit has no effect. A read from this register will be **undefined**. The INTCLR signal is a "one shot" event. That is, the INTCLR signal is transitory; when a ‘1’ is written the latch is cleared immediately. On the next IP clock cycle the latch is ready for a new interrupt. Returning the INTCLR bit to ‘0’ after clearing is not necessary.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I8	I7	I6	I5	I4	I3	I2	I1	-	-	TH	AX	TI	M12	P12	P05

3.5.5 INTPEN: The Interrupt Pending Register (I/O Address 1A)

Read register 16 bits

This is a read-only register that indicates the contents of the interrupt latches. A ‘1’ Indicates that the latch has been set. A ‘0’ indicates that the latch is clear and no interrupt is pending. Note: this register shows the contents of the latch not the interrupt source status. Use INTD to monitor the instantaneous source state.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
I8	I7	I6	I5	I4	I3	I2	I1	-	-	TH	AX	TI	M12	P12	P05

3.5.6 VECTOR: The Interrupt Vector Register (I/O Address 1C)

Write register 8 bits

The Interrupt Vector Register is an 8 bit vector that is returned on the data bus when the IP carrier asserts the INTSEL* signal during interrupt servicing. The six most significant bits of the interrupt vector, V7 through to V2, are user programmable. The two least significant bits V0 & V1 indicate the interrupt source group.
If the user portion of the vector has not been initialised the vector will return 0x0F the 68k family code for Un-initialised Interrupt Vector.

Source	IP IRQ Level	V7 to V0
I/O1	0	xxxxxx00
I/O2	0	xxxxxx00
I/O3	0	xxxxxx00
I/O4	0	xxxxxx00
I/O5	0	xxxxxx00
I/O6	0	xxxxxx00
I/O7	0	xxxxxx00
I/O8	0	xxxxxx00
Thermostat	1	xxxxxx01
Timer Time Out	1	xxxxxx01
+5 Volt Monitor	1	xxxxxx10
+12 Volt Monitor	1	xxxxxx10
-12 Volt Monitor	1	xxxxxx10
Aux Pwr Monitor	1	xxxxxx10
Un-initialised	either	00001111

4. ID PROM

The 8530 IP module includes a configuration ID PROM. The ID information held in the PROM is as detailed below.

The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'I'	49h
Base+82	ASCII 'P'	50h
Base+84	ASCII 'A '	41h
Base+86	ASCII 'C '	43h
Base+88	Manufacturer ID	F0h
Base+8A	Model number	54h
Base+8C	Revision	A1h
Base+8E	Reserved	00h
Base+90	Driver ID Lo Byte	01h
Base+92	Driver ID Hi Byte	00h
Base+94	No of bytes used	0Ch
Base+96	CRC	3Ch

APPENDIX A (I/O Pin Wiring)

I/O Connector – 50 way on 8530\8630 Watchdog Board

Pin	Signal	Description
1	IO1	I/O Line 1
2	GND	
3	IO2	I/O Line 2
4	GND	
5	IO3	I/O Line 3
6	GND	
7	IO4	I/O Line 4
8	GND	
9	IO5	I/O Line 5
10	GND	
11	IO6	I/O Line 6
12	GND	
13	IO7	I/O Line 7
14	GND	
15	IO8	I/O Line 8
16	GND	
17	THSO	Thermostat Status Output
18	GND	
19	AUXSO	Aux. voltage Mon Status Output
20	GND	
21	PO5SO	+5 volt Monitor Status Output
22	GND	
23	P12SO	+12 volt Monitor Status Output
24	GND	
25	M12SO	-12 volt Monitor Status Output
26	GND	
27	TIZSO	Timer = Zero Status Output
28	GND	
29	FP05	Fused +5 volt monitor Input
30	GND	
31	TIPSO	Timer Periodic Output
32	GND	
33	P24	Auxiliary +24 volt tap
34	GND	
35	P48	Auxiliary +48 volt tap
36	GND	
37	M24	Auxiliary -24 volt tap
38	GND	
39	M48	Auxiliary -48 volt tap
40	GND	
41	FP12	Fused +12 volt monitor Input
42	GND	
43	FM12	Fused -12 volt monitor Input
44	GND	
45	FVREF5	5 volt Precision Reference
46	GND	
47	VREF2	2 volt Precision Reference
48	GND	
49	SYSRESET*	VMEbus SYSRESET*
50	GND	

Note
FVREF5 and VREF2 are test points for the precision voltage sources used in the power monitor circuits.

APPENDIX B (50Way Pin Wiring on Hytec transition Card 8304)

I/O Connector – 50 way on Hytec transition Card 8304 where this feeds ONE IP sites

Pin Trans	Pin 8522	Signal	Pin Trans	Pin 8522	Signal
1	*2*	GND	**26**	*1*	IO1
2	*4*	GND	**27**	*3*	IO2
3	*6*	GND	**28**	*5*	IO3
4	*8*	GND	**29**	*7*	IO4
5	*10*	GND	**30**	*9*	IO5
6	*12*	GND	**31**	*11*	IO6
7	*14*	GND	**32**	*13*	IO7
8	*16*	GND	**33**	*15*	IO8
9	*18*	GND	**34**	*17*	THSO
10	*20*	GND	**35**	*19*	AUXSO
11	*22*	GND	**36**	*21*	PO5SO
12	*24*	GND	**37**	*23*	P12SO
13	*26*	GND	**38**	*25*	M12SO
14	*28*	GND	**39**	*27*	TIZSO Timer = Zero Status Output
15	*30*	GND	**40**	*29*	FP05
16	*32*	GND	**41**	*31*	TIPSO Timer Periodic Output
17	*34*	GND	**42**	*33*	P24
18	*36*	GND	**43**	*35*	P48
19	*38*	GND	**44**	*37*	M24
20	*40*	GND	**45**	*39*	M48
21	*42*	GND	**46**	*41*	FP12
22	*44*	GND	**47**	*43*	FM12
23	*46*	GND	**48**	*45*	FVREF5
24	*48*	GND	**49**	*47*	VREF2
25	*50*	GND	**50**	*49*	SYSRESET*

Note
FVREF5 and VREF2 are test points for the precision voltage sources used in the power monitor circuits.

APPENDIX C (Circuit diagram)

The circuit diagram below is for reference only.