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IP-DIO-8606
48-bits Digital I/O Board
INDUSTRY PACK

USERS MANUAL

Document No: 8606/UTM/G/X1.0
Date: 01/10/2019

Author: MRN

Revision History

The following table shows the revision history for this document.

Date	Version	Change Notes
01/10/2019	1.0	Issued

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1. INTRODUCTION

This is a single-width IP module with forty eight channels of buffered digital input/output.
The I/O signals are accessed in to six groups of 8-bits or three groups of 16-bits. Each group of eight/sixteen signals can be selected to be inputs or outputs. At power-up or after an IP reset, all signals default to the input state.
A control register associated with the I/O register determines whether each group will act as inputs or outputs. It also controls the way that inputs are sampled for input mode.
When output mode is selected, the output data reflects the last data written to the corresponding I/O register. The buffered TTL outputs can be programmed to be steady levels or pulses with positive true or false states.
When input mode is selected other control register bits come into play and determine the sampling mode of the register. One common sampling clock can be selected from a choice of four in the range 1kHz to 1MHz. Also, a common de-bounce clock can be chosen from the following frequencies: 100Hz, 200Hz, 500Hz and 1kHz.
Writing to a group when input mode is selected has no effect.
Reading the group when output mode is selected will read back the last data written.
A pulse parameter register determines the duration of pulsed outputs up to 100 seconds.
A further register associated with each group controls which bits may generate an interrupt when in input mode. [Again, this function has no effect when in output mode.]
All the above registers occupy I/O space on the IP card in three groups, starting at offset zero+a (where a = 00, 20 or 40 Hex) as follows:

Offset	Name	Description
a+0	LKC	Last Known Change/Data Register
a+2	CSR	Control and Status Register
a+4	IMR	Mask Register
a+6	DBR	Debounce Register
a+8	PSR	Pulse Select Register
a+A	PPR	Pulse Parameter Register
a+C	IRV	Interrupt Request Vector

2. PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of input/outputs:	48 (configurable as 3 groups of 16 in or 16 out)
Input level:	TTL
Output level	TTL 24mA, programmable logic sense high or low true
Input/output termination:	4k7 ohms to 0V, or +3.3V or 5V by jumpered selection
Internal clock:	50MHz oscillator.
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 250mA typical

3. OPERATING MODES

There are several basic operating modes set according to the CSR (see below):-

4. APPLICATION REGISTERS

There are 3 groups of 7 application (I/O) registers described by address offset a=0x00, 0x20 and 0x40.

4.1 Last Known Change/Data Register LKC IP Address 0 (Read/Write)

Address: Base +a + 0x0

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LKC15	LKC14	LKC13	LKC12	LKC11	LKC10	LKC9	LKC8	LKC7	LKC6	LKC5	LKC4	LKC3	LKC2	LKC1	LKC0

This register shows the last known state of the I/O data. In the case of inputs it shows the input states conditioned by de-bounce and change-of-state detection. For outputs, the new data should be written here.

4.2 Control/Status Register CSR IP Address 1 (Read/Write)

Address: Base +a+ 0x2

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
COS BIT	IO INT EN	PL			OM				SCAN T1	SCAN T0	COS T1	COS T0			SCAN EN

SCAN EN Start scanning digital inputs
COS T0-T1 De-bounce clock frequency select:

CSR I/O		Debounce Scan rate	
Bit 4	**Bit 3**	**Internal Clock**	**Ext/Strobe clock**
0	0	100Hz	Div 10000
0	1	200Hz	Div 5000
1	0	500Hz	Div 2000
1	1	1KHz	Div 1000

SCAN T0-T1 Select scan rate of digital inputs:

CSR I/O		Scan Rate	
Bit 6	**Bit5**	**Internal Clock**	**Ext/Strobe clock**
0	0	1KHz	Div 1000
0	1	10KHz	Div 100
1	0	100KHz	Div 10
1	1	1MHz	Div 1

OM Enable digital lines: '0' = all inputs; '1' = all outputs;
PL Set I/O logic sense: '0' = +ve logic; '1' = -ve logic;
IO INT EN Enable interrupts to be generated by a change of state of the IO inputs.
COS BIT This bit signifies a change of state which causes an interrupt to be generated. A '0' needs to be written to this bit to clear the interrupt.

4.3 Digital Input Interrupt Mask Register IMR IP Address 2 (Read/Write)

Address: Base +a+ 0x4

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

The mask register only acts on input signals. Writing a '1' to a bit will allow a change-of-state on the corresponding input to generate an interrupt. Any output bits that have a corresponding '1' in this register will not generate interrupts.

4.4 De-bounce Register DBR IP Address 3 (Read/Write)

Address: Base +a+ 0x6

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

The de-bounce register only applies to bit selected as inputs. A '1' written to a bit position causes that input to be de-bounced at the selected common clock rate

4.5 Pulse Select Register PSR IP Address 4(Read/Write)

Address: Base +a+ 0x8

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

The Pulse Select register only applies to bit selected as outputs. Writing a '1' to a bit makes the corresponding output a pulsed type. In this case, writing a '1' to a bit in the LKC/Data register will cause the corresponding output to produce a pulse of a width controlled by the Pulse Parameter Register. At the end of the pulse, the corresponding bit in the LKC/Data register will be cleared.

4.6 Pulse Parameter Register PPR IP Address 5 (Read/Write)

Address: Base +a+ 0xA

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
PP15	PP14	PP13	PP12	PP11	PP10	PP9	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

The pulse parameter register controls the width of the output pulse produced when the corresponding bit is written as a '1' in the data register. The function of the bits are as follows:

Width	**PP4**	**PP3**	**PP2**	**PP1**	**PP0**
1 msec	0	0	0	0	0
10 msec	0	0	0	0	1
100 msec	0	0	0	1	0
1 second	0	0	0	1	1
2 seconds	0	0	1	0	0
5 seconds	0	0	1	0	1
10 seconds	0	0	1	1	0
20 seconds	0	0	1	1	1
50 seconds	0	1	0	0	0
100 secs	0	1	0	0	1

All other bits – no effect.

4.7 Vector IRV IP address 6 (Read/Write)

Address: Base +a+ 0xC
Sets the interrupt request vector read by interrupt select.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

5. ID PROM

The ID configuration information held in the PROM is as detailed below.
The byte addresses of the ID PROM are as below:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	ID high byte	0080h	
Base+88	ID low word	0300h	
Base+8A	Model number	8606h	
Base+8C	Revision	0101h	(This shows PCB Issue 1 and FPGA at issue 1)
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Not used	xxxxxh	
Base+9A	Serial Number	xxxxd	

6. Jumpers

J1	2-4	Terminate data I/O lines to Gnd
	2-1	Terminate data I/O lines to 3.3V
	2-3	Terminate data I/O lines to 5V
J2, J3 and J4		Not Used in this design

7. I/O Connector – 50 way on 8606 Board

Pin	Signal	Pin	Signal
1	I/O 1	26	I/O 26
2	I/O 2	27	I/O 27
3	I/O 3	28	I/O 28
4	I/O 4	29	I/O 29
5	I/O 5	30	I/O 30
6	I/O 6	31	I/O 31
7	I/O 7	32	I/O 32
8	I/O 8	33	I/O 33
9	I/O 9	34	I/O 34
10	I/O 10	35	I/O 35
11	I/O 11	36	I/O 36
12	I/O 12	37	I/O 37
13	I/O 13	38	I/O 38
14	I/O 14	39	I/O 39
15	I/O 15	40	I/O 40
16	I/O 16	41	I/O 41
17	I/O 17	42	I/O 42
18	I/O 18	43	I/O 43
19	I/O 19	44	I/O 44
20	I/O 20	45	I/O 45
21	I/O 21	46	I/O 46
22	I/O 22	47	I/O 47
23	I/O 23	48	I/O 48
24	I/O 24	49	GND
25	I/O 25	50	GND

8600 Pin	Buffer IC	FPGA Pin	8606 IP Signal	Transition Card Pin	8600 Pin	Buffer IC	FPGA Pin	8600 IP Signal	Transition Card Pin
1	6	D13	I/O1	26	26	11	E10	I/O	13
2	12	C8	I/O2	1	27	10	B4	I/O	39
3	6	C13	I/O3	27	28	11	D10	I/O	14
4	12	D8	I/O4	2	29	10	A3	I/O	40
5	6	B15	I/O5	28	30	11	D11	I/O	15
6	12	C10	I/O6	3	31	10	B3	I/O	41
7	6	B14	I/O7	29	32	11	C12	I/O	16
8	12	D9	I/O 8	4	33	9	C11	I/O	42
9	6	A14	I/O9	30	34	13	F16	I/O	17
10	12	K16	I/O10	5	35	9	A11	I/O	43
11	6	A13	I/O11	31	36	13	F14	I/O	18
12	12	J16	I/O12	6	37	9	B10	I/O	44
13	6	B12	I/O13	32	38	13	C15	I/O	19
14	12	J14	I/O14	7	39	9	A10	I/O	45
15	6	A12	I/O15	33	40	13	B8	I/O	20
16	12	H14	I/O16	8	41	9	C9	I/O	46
17	10	A6	I/O	34	42	13	H16	I/O	21
18	11	F8	I/O	9	43	9	A9	I/O	47
19	10	B6	I/O	35	44	13	H15	I/O	22
20	11	E7	I/O	10	45	9	A7	I/O	48
21	10	A5	I/O	36	46	13	F15	I/O	23
22	11	C6	I/O	11	47	9	C7	I/O	49
23	10	C5	I/O	37	48	13	E16	I/O	24
24	11	D7	I/O	12	49	-		GND	50
25	10	A4	I/O	38	50	-		GND	25

8. TRANSITION BOARD CONNECTIONS

TB 8304 I/O Connector – Straight through connection transition board. With 4 x 50-way SCSI-2 connectors

Pin Assignments 50-way SCSI-2 connectors

Pin	Signal	Pin	Signal
1	I/O2	26	I/O1
2	I/O4	27	I/O3
3	I/O6	28	I/O5
4	I/O8	29	I/O7
5	I/O10	30	I/O9
6	I/O12	31	I/O11
7	I/O14	32	I/O13
8	I/O16	33	I/O15
9	I/O18	34	I/O17
10	I/O20	35	I/O19
11	I/O22	36	I/O21
12	I/O24	37	I/O23
13	I/O26	38	I/O25
14	I/O28	39	I/O27
15	I/O30	40	I/O29
16	I/O32	41	I/O31
17	I/O34	42	I/O33
18	I/O36	43	I/O35
19	I/O38	44	I/O37
20	I/O40	45	I/O39
21	I/O42	46	I/O41
22	I/O44	47	I/O43
23	I/O46	48	I/O45
24	I/O48	49	I/O47
25	GND	50	GND

Pin	IC	FPGA Pin	Signal		Pin	IC	FPGA Pin	Signal
1	12	C8	I/O2		26	6	D13	I/O1
2	12	D8	I/O4		27	6	C13	I/O3
3	12	C10	I/O6		28	6	B15	I/O5
4	12	D9	I/O8		29	6	B14	I/O7
5	12	K16	I/O10		30	6	A14	I/O9
6	12	J16	I/O12		31	6	A13	I/O11
7	12	J14	I/O14		32	6	B12	I/O13
8	12	H14	I/O16		33	6	A12	I/O15
9	11	F8	I/O		34	10	A6	I/O
10	11	E7	I/O		35	10	B6	I/O
11	11	C6	I/O		36	10	A5	I/O
12	11	D7	I/O		37	10	C5	I/O
13	11	E10	I/O		38	10	A4	I/O
14	11	D10	I/O		39	10	B4	I/O
15	11	D11	I/O		40	10	A3	I/O
16	11	C12	I/O		41	10	B3	I/O
17	13	F16	I/O		42	9	C11	I/O
18	13	F14	I/O		43	9	A11	I/O
19	13	C15	I/O		44	9	B10	I/O
20	13	B8	I/O		45	9	A10	I/O
21	13	H16	I/O		46	9	C9	I/O
22	13	H15	I/O		47	9	A9	I/O
23	13	F15	I/O		48	9	A7	I/O
24	13	E16	I/O48		49	9	C7	I/O47
25	-	-	GND		50	-	-	GND